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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,245	07/11/2001	Debra M. Bell	303.751US1	9496

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EXAMINER	
WONG, LINDA	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,245	BELL, DEBRA M.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/11/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 13-17* is/are allowed.

6)☒ Claim(s) *1-8,10,18-23,25-31 and 34-44* is/are rejected.

7)☒ Claim(s) *11-12,24,and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/11/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the following

   a. In Fig 1, labels for 122, 124, 126 should be included in the diagram.

   b. In Fig. 1, a label for 151-154 should be included in the diagram.

   c. In Fig. 4, a label for box 412 or units contained in box 412, labeled 413-0 – 413-N, should be included in the diagram.

   d. In Fig. 4, a label for box 405 or units contained in box 405, labeled 410-0 – 410-N, should be included in the diagram.

   e. In Fig. 5, labels for 122, 124, 126 should be included in the diagram.

   f. In Fig. 5, a label for 151-154 should be included in the diagram.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 18, line 1, the phrase "has been disclosed DLL" is suggested to be changed to "has been disclosed." Appropriate correction is required.

Claim Objections

3. Claim 20 is objected to because of the following informalities: the end of the claim should contain a ".", as opposed to a ",". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claim 30 recites the limitation of the "processor" and "memory device" in claim 27. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1-3,7-8,10,18,20-23,25-28,30-31,33-38,42-44 are rejected under 35 USC 102(b) as being unpatentable over Baker et al. (US Patent No: 6445231)

   a. Regarding **claim 1**, Baker et al disclose a coarse delay segment (coarse loop Fig 2A, label 205a) outputs a coarse delayed signal and a fine delay segment (Fig. 2A, label 205b), which receives a coarse delayed signal to generate an output. Baker et al also disclose in Fig. 2A a coarse delay output, 211, is

inputted into the fine delay segment, wherein the fine delay, feedback 212, is adjusted by the coarse delay. The fine delay segment adjusts the fine delay based on the shifting signals shown in Fig. 9.

b. Regarding **claim 2,** Baker et al disclose a coarse delay segment (Fig. 2A, label 205a) provides wide frequency lock range and a fine delay segment that provides tight locking. (Col. 1, lines 64-67 and Col. 2, lines 1-2)

c. Regarding **claim 3,** Baker et al also disclose that each of the delay stages in the fine delay segment (Fig. 9) has a "substantially smaller" delay "than that of "each of the delay stages of the coarse loop." (Col. 8, lines 19-21)

d. Regarding **claim 7**, Baker et al. disclose a coarse delay segment (coarse loop Fig 2A, label 205a) and a fine delay segment containing a plurality of delay signals (Fig. 9, label 918-1 – 918-N), a phase detector (Fig. 3A, label 302), an output from the fine delay segment that depends on the shift register (Fig. 9, label 908 and 918-1 – 918-N) and a logic circuit connected to a register control that receives the shifting signals to determine whether the delay should be adjusted. (Fig. 5A, label 308)

e. Regarding **claim 8**, Baker et al disclose a fine delay segment (fine loop, Fig. 2A) that switches between the minimum (delay cell Fig. 5A, label 520-1) and maximum (delay cell Fig. 5A, label 520-N) amount of delay by turning on the delay cells until the inputs are synchronized. (Fig. 5A and Cols. 5 and 6, lines 60-67 and lines 1-5)

f. Regarding **claim 10**, Baker et al disclose a delay line containing a plurality of delay stages in a coarse loop (Fig. 3A, label 310) and a controller connected to a logic circuit and delay line. The controller receives inputs from the shifting signals to determine the delay adjustment. (register controller in Fig. 5A, label 515).

g. Regarding **claim 18**, Baker et al disclose a main memory containing plurality of memory cells and an output circuit connected to the main memory. (Col. 3, lines 11-23) A DLL connected to the output circuit. (Col. 3, lines 31-35) Claim 1 encloses the limitations of the DLL.

h. Regarding **claim 20 and 21**, Baker et al disclose a data bus connected to the output circuit and main memory, comprised of memory cells. (Col. 3, lines 21-23 and lines 12-19) In Fig. 2a, Baker et al shows the DLLout as an input to the output circuit. (Fig. 2A, label 212) The CLKout, equivalent to DS, is synchronized with the data signal, DQ. (Col. 4, lines 8-10) Baker et al depicts in Fig. 2A, an external clock, CLKin, which is synchronized to CLKout, the output from the DLL and output model. The data signal, DQ, is synchronized with DS, which inherently indicates that the external clock is synchronized with the data signal. (Col. 4, lines 8-30)

i. Regarding **claim 22,** Baker et al disclose a model circuit that is "identical to output circuit". (Col. 4, lines 3-4) As depicted in Fig. 2A, the model circuit (output model Fig. 2A, label 216) is connected to the fine delay segment (fine loop Fig 2A, label 205b).

j. Regarding **claim 23**, Baker et al (US Patent No: 6445231) disclose a main memory with plurality of memory cells along with an output circuit connected to the memory cell. (Col. 3, lines 8-30) Claim 7 encloses all the limitations of the DLL claimed.

k. **Claim 25** inherits all the limitations of claim 21.

l. **Claim 26** inherits all the limitations of claim 21.

m. **Claim 27** inherits all the limitations of claim 22.

n. Regarding **claim 28**, Baker et al include a processor connected to the memory device and inherit all the limitations of claim 18. (Col. 10, lines 7-8)

o. Regarding **claim 30**, Baker et al disclose a data bus connected between the processor and the memory device and inherits all the limitations of claim 21. (Col. 10, lines 7-8)

p. Regarding **claim 31**, Baker et al teach a processor connected to the memory device, which comprises of a plurality of memory cells, and inherits all the limitations of claim 28. (Col. 10, lines 7- 8)

q. Regarding **claim 33**, Baker et al include a data bus connected between the processor and the memory device (Fig. 15) and inherit all the limitations of claim 21.

r. Regarding **claim 34**, Baker et al depict a clock input delayed by a coarse delay in the coarse delay segment (Fig. 2A, label 205a), fine delay segment receiving an input from the coarse delay segment to output a fine delayed signal (Fig. 2A, label 211), a shifting register controlled by the output of the

phase detector, which detects the difference between CLKin and CLKout (Fig. 3A), a register controller, which controls the shifting of the delay line of the coarse and fine delay (Fig. 5A). Although Baker et al does not disclose that the coarse delay is shifted based on the fine delay, Keeth et al disclose that the coarse delay is shifted when the fine delay has reached a predetermined maximum or minimum. (Col. 5, lines 9-17)

s. **Claim 35** inherits all the limitations of claim 7.

t. **Claim 36** inherits all the limitations of claim 2.

u. **Claim 37** inherits all the limitations of claim 3.

v. **Claim 38** encloses all the limitations of claim 3.

w. Regarding **claim 42**, Baker et al disclose a coarse delay segment (coarse loop Fig. 2A, label 205a) that applies a coarse delay (Col. 3, lines 52-53), a fine delay segment that applies a fine delay (Col. 3, lines 54-55), both comprised of a plurality of coarse and fine delay signals, respectively (fine loop fig. 2A, label 205b and Fig. 9, label 910), a feedback from the fine delay that is adjusted by the coarse delay segment (Fig. 2A), a shift register that controls and selects the next delay or output (Col. 4, lines 60-61), a phase detector that generates a difference in phase between two inputs, and the shift register detects when to adjust the coarse and fine delay segments accordingly. (Fig. 5A)

x. **Claim 43** inherits all the limitations of claim 2.

y. Regarding **claim 44**, Baker et al disclose a shift register receiving inputs from a phase detector and based on the signals from the phase detector, the shift register controls and selects the next delayed signal. (Fig. 9 and Col. 8,lines 15-34)

Claim Rejections - 35 USC § 103

6. Claim 4-6,9,19,29,39-41 are rejected under 35 USC 103 as being unpatentable over Baker et al (US Patent No: 6445231) in view of Keeth et al (US Patent No: 6101197).

a. Regarding **claim 4 and 5**, Baker et al disclose a shifting register that controls the amount of delay (Baker 4, lines 60-62), but does not teach how the coarse delay and fine delay are adjusted. Keeth et al disclose a coarse delay (within coarse delay circuit Fig 2, label 158) adjusted "whenever the maximum or minimum delay of the fine delay circuit" is reached. (Abstract, lines 12-14) Keeth et al also disclose that the coarse delay is decreased when the fine delay circuit within the range of the predetermined fine delay minimum and increased when the fine delay segment is within the range of the predetermined maximum. (Col. 5, lines 9-17) By adjusting the coarse delay and fine delay, it would be obvious to one skilled in the art to use this method to provide better synchronization.

b. **Claim 6** inherits all the limitations of claims 4 and 5.

c. Regarding **claim 9**, as explained in the rejection of claim 8, Keeth et al indicates an adjustment of coarse delay range and fine delay range in the coarse delay circuit and fine delay circuit. (Abstract, lines 12 –14)

d. **Claim 19** inherits all the limitations of claims 4 and 5.

e. **Claim 29** inherits all the limitations of claims 4 and 5.

f. **Claim 39** inherits all the limitations of claim 6.

g. **Claim 40** inherits all the limitations of claims 4 and 5.

h. **Claim 41** inherits all the limitations of claims 4 and 5.

Allowable Subject Matter

7. **Claims 11-12, 24, and 32** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. **Claims 13-17** are allowable over prior art of record. The following is an examiner's statement of reasons for allowance: the teachings of a selector connected to the fine delay paths to select one of the fine delayed signals based on select signals to provide an internal clock signal is not taught by a prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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